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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/762,013

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Michihisa Maeda

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07/25/2006

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EXAMINER

NOVACEK, CHRISTY L

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 07/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/762,013	Applicant(s) MAEDA ET AL.	
	Examiner Christy L. Novacek	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to the amendment and request for continued examination filed July 10, 2006.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 10, 2006 has been entered.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 3, 4 and 7-13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Yagi et al. (US 6,109,507, previously cited) and Kimura et al. (US 6,400,034, previously cited).

Regarding claim 1, Applicant's own admitted prior art discloses applying a no-clean flux to a first surface of a substrate having solder bumps attached thereto. The solder bumps are aligned and brought into contact with corresponding metal bumps that are attached to a first surface of a chip. The solder bumps are heated to a first temperature that is equal or greater to the melting temperature of the solder bumps. The admitted prior art discloses using a flux, which does not have a volatilization temperature less than the melting temperature (paragraphs 0004-

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0006). Like the admitted prior art, Yagi discloses a process of applying solder and flux to a substrate and using heat to attach the solder to the substrate. Yagi discloses that it is advantageous for the flux to have a volatilization temperature less than the melting point of the solder because that way, voids in the solder ball caused by trapped air bubbles can be prevented (col. 13, ln. 24-31). At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute the flux of Yagi in the invention of the admitted prior art because Yagi's flux leaves behind no undesirable voids in the solder balls, thus improving the reliability of the bond between the chip and the substrate.

Further regarding claim 1 and claims 3, 4 and 7-13, Applicant's admitted prior art does not disclose a method for heating the solder bumps and joining the chip to the substrate. Like the admitted prior art, Kimura discloses a process of flip-chip bonding a substrate to a chip wherein metal contacting the chip and substrate is used to bond the chip and substrate together. Kimura teaches using a thermo-compression bonding tool to effect the flip-chip bonding. By this method, the substrate is attached to a lower platen that is maintained at a temperature of 70°C, the chip is attached to a heater which applies both heat (at a temperature of 300°C) and a pressure (at a force of 75-125 gf/bump) to a second surface of the chip whereby the heat is conducted through the chip such that the metal becomes bonded to both the chip and the substrate. The heat and pressure are applied to the chip for a time period of 2.5-7.5 seconds to conduct the bonding and then the contact force is removed (col. 6, ln. 64 – col. 7, ln. 35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the thermo-compression bonding method of Kimura to effect the bonding of the chip to the substrate of the admitted prior

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art because the Kimura teaches that using his particular thermo-compression process, a chip can be bonded to a substrate with reduced heat and pressure application.

Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Yagi et al. (US 6,109,507) and Kimura et al. (US 6,400,034), as applied to claim 1 above, and further in view of Hur et al. (US 6,013,572, previously cited).

Regarding claim 2, Applicant's admitted prior art does not disclose the materials that make up the first surface of the chip. Like the admitted prior art, Hur discloses a method of bonding a chip to a substrate using solder bumps. Hur teaches that a chip surface having bonding pads including copper can provide strong adhesiveness to the chip and is strong enough to withstand damage during subsequent processing (col. 3, ln. 60 – col. 4, ln. 14; col. 6, ln. 56-67). Hur also teaches that methods of manufacturing this type of bonding pad are well-known in the art (col. 4, ln. 12-14). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the bonding pads on the surface of the chip of the admitted prior art such that they are the copper-containing bonding pads of Hur because the admitted prior art does not disclose any particular bond pad material and Hur teaches that a bond pad including copper has strong adhesiveness and increased durability.

Regarding claim 5, Applicant's admitted prior art discloses that conventional solder is made of 97% Pb and 3% Sn. Like the admitted prior art, Hur discloses a method of bonding a chip to a substrate using solder bumps. Hur teaches a method whereby the solder bumps are comprised of 96.5% Sn and 3.5% Ag (col. 7, ln. 42-43). Hur states that the Sn/Ag solder bumps are advantageous over the conventional Pb/Sn solder bumps because lead is harmful to the

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environment (col. 1, ln. 35-47). At the time of the invention, it would have been obvious to one of ordinary skill in the art to replace the Pb/Sn solder balls of the admitted prior art with the Sn/Ag solder balls disclosed by Hur because Hur teaches that it is advantageous to use Sn/Ag solder balls instead of Pb/Sn solder balls because lead is harmful to the environment.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Yagi et al. (US 6,109,507) and Kimura et al. (US 6,400,034), as applied to claim 1 above, and further in view of Arbib (EP 0077622, previously cited).

Regarding claim 6, Yagi discloses that it is beneficial to use a flux that has a lower boiling point than the melting point of the solder, but Yagi does not disclose any particular flux. Like Yagi, Arbib discloses using a flux to assist in the bonding of electronic components and also teaches that the flux should have a lower boiling point than the soldering temperature. Arbib discloses that this type of flux preferably comprises a flux material having at least one carboxylic acid group (Abstract). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the flux of Arbib to do the solder bonding disclosed in the admitted prior art because both Yagi and Arbib teach using a flux that has boiling point below the soldering temperature and Arbib discloses that this type of flux can successfully be made using a flux material having at least one carboxylic acid group. It would also have been obvious to one of ordinary skill in the art to use routine experimentation to determine an optimal boiling point of the flux, depending upon the type of solder being used because such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955).

Response to Arguments

Applicant's arguments filed July 10, 2006 have been fully considered but they are not persuasive.

Regarding the rejection of claim 1, Applicant alleges that neither the admitted prior art nor Yagi disclose a no-clean flux. Firstly, Applicant's own definition of "no-clean flux", as provided on page 6, paragraph 0017 of the specification, states, "a no-clean flux is one that includes constituents that completely volatilize at a specific temperature, leaving no solid residue." Applicant's own prior art admits, "Fluxes have been developed which completely volatilize at elevated temperature." (pg. 4, para. 0006). Furthermore, Applicant's own prior art states, "In typical [prior art] C4 bonding processes, fluxes serve an additional purpose of adhesively holding the chip and substrate together until the re-flow temperature was reached during joining. Accordingly, even no-clean fluxes used in the C4 process [of the prior art] have constituents that have boiling points above the melting points of the solder bumps." (pg. 9, para. 0024). Hence, Applicant's admitted prior art recites the use of no-clean fluxes. Additionally, Yagi states, "Generally, the melting point of the solder particle is higher than the evaporation point of the flux. Thus, after the air at the surface of the pad 12 has escaped out of the solder paste 22, the particles will melt and join with the pad 12. Then, there will be no air existing at the surface of the pad 12." Yagi does not disclose that there is any flux residue left behind after the evaporation and Yagi does not disclose that any cleaning step is required to remove flux residue. Therefore, Yagi also suggests using a no-clean flux.

Also regarding the rejection of claim 1, Applicant alleges that the prior art fails to disclose using a thermo-compression bonder. Kimura, previously cited, discloses a method of

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bonding solder bumps with metal bumps using a thermo-compression bonder to apply heat and pressure to melt and join the bumps. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the thermo-compression bonding method of Kimura to effect the bonding of the chip to the substrate of the admitted prior art because the Kimura teaches that using his particular thermo-compression process, a chip can be bonded to a substrate with reduced heat and pressure application.

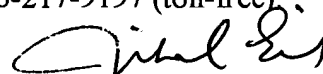
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
July 20, 2006



Michael Trinh
Primary Examiner